WHAT IS CLAIMED IS:

1. A universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out (FIFO) buffer;

a circuit for detecting a last word transmitted from said FIFO buffer;

a transmitter empty circuit for generating a transmitter empty signal on a transmitter empty control line when a last word transmitted from said FIFO buffer is detected;

a delay circuit for delaying generation of said transmitter empty signal for a programmable delay time; and

a programmable register for setting said programmable delay time.

2. The UART of claim 1 wherein said transmitter empty signal is an internal signal triggered from a stop bit of said last word.

3. The UART of claim 1 wherein said programmable register comprises a shadow register which is a write-only portion of a register only read by a user.

4. The UART of claim 3 wherein said write-only portion comprises the first 4 bits of a modem status register.

5. The UART of claim 1 wherein said programmable register is a four bit register.

6. The UART of claim 1 further comprising:

a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and

said delay circuit and said programmable register being a single circuit and register connected to control the delay of said transmitter empty signal for each of said channels.

7. ~~A~~ universal asynchronous receiver transmitter (UART) comprising:

a first-in, first-out ~~(FIFO)~~ buffer;

a circuit for detecting a last word transmitted from said FIFO buffer;

a transmitter empty circuit for generating a transmitter empty signal on a transmitter empty control line when a last word transmitted from said FIFO buffer is

detected, wherein said transmitter empty signal is an internal signal triggered from a stop bit of said last word;

a delay circuit for delaying generation of said transmitter empty signal for a programmable delay time;

a programmable register for setting said programmable delay time, wherein said programmable register comprises a shadow register which is a write-only portion of a register only read by a user;

a plurality of channels, each channel having said FIFO buffer, said circuit for detecting a last word and said transmitter empty circuit; and

said delay circuit and said programmable register being a single circuit and register connected to control the delay of said transmitter empty signal for each of said channels.

8. The UART of claim 3 wherein said write-only portion comprises the first 4 bits of a modem status register.

9. The UART of claim 1 wherein said programmable register is a four bit register.

10. The UART of claim 7 further comprising at least 8 of said channels.